



DE-DOCKETED

UNITED STATES PATENT AND TRADEMARK OFFICE

108298532US1
ptp/ISW

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
PO. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPL NO.	FILING OR 371 (c) DATE	ART UNIT	FIL FEE REC'D	ATTY.DOCKET NO	DRAWINGS	TOT CLMS	IND CLMS
10/620,714	07/15/2003	2833	1254	108298532US1	3	34	6

25096
PERKINS COIE LLP
PATENT-SEA
P.O. BOX 1247
SEATTLE, WA 98111-1247

RECEIVED

OCT 20 2003

PERKINS COIE LLP

CONFIRMATION NO. 9586
FILING RECEIPT



OC000000011038012

Date Mailed: 10/15/2003

Receipt is acknowledged of this regular Patent Application. It will be considered in its order and you will be notified as to the results of the examination. Be sure to provide the U.S. APPLICATION NUMBER, FILING DATE, NAME OF APPLICANT, and TITLE OF INVENTION when inquiring about this application. Fees transmitted by check or draft are subject to collection. Please verify the accuracy of the data presented on this receipt. If an error is noted on this Filing Receipt, please write to the Office of Initial Patent Examination's Filing Receipt Corrections, facsimile number 703-746-9195. Please provide a copy of this Filing Receipt with the changes noted thereon. If you received a "Notice to File Missing Parts" for this application, please submit any corrections to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections (if appropriate).

Applicant(s)

David J. Corisis, Nampa, ID;

Domestic Priority data as claimed by applicant

This application is a DIV of 09/644,766 08/23/2000 PAT 6,607,937

Foreign Applications

If Required, Foreign Filing License Granted: 10/15/2003

Projected Publication Date: 01/22/2004

Non-Publication Request: No

Early Publication Request: No

Title

Stacked microelectronic dies and methods for stacking microelectronic dies

Preliminary Class